1. A yield enhancement circuit for substituting a redundant circuit for a faulty circuit of an integrated circuit, comprising:

a plurality of fault indication devices, wherein each fault indication device is associated with one sub-circuit of the integrated circuit such that one fault indication device is activated to generate a fault signal to express existence of a fault within the faulty circuit of said integrated circuit, additionally each fault indication device that is associated with selected adjacent sub-circuits of the integrated circuit activates the fault signal to express existence of the fault within the faulty circuit of said integrated circuit;

a fault detection device in communication with the plurality of fault indication devices to determine the existence of the faulty circuit within the integrated circuit and transmit a redundancy implementation signal upon determination of existence of the faulty circuit; and

a plurality of redundancy activation circuits in communication with the fault detection device to receive the redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the sub-circuit to which said fault indication device is associated and to which said fault indication device selectively transfers input/output signals of the sub-circuit associated with the fault indication device and its adjacent sub-

circuit to a designated path dependent on the expression of the existence of a fault within the integrated circuit.

2. The yield enhancement circuit of claim 1 wherein if the fault indication device is not activated indicating that the associated sub-circuit has no fault and the redundancy implementation signal indicates that no fault exists in said integrated circuit, the input/output signals of said circuit are transferred to their designated path.

3. The yield enhancement circuit of claim 1 wherein if the fault indication device is not activated indicating that the associated circuit has no fault, but the redundancy implementation signal indicates that the fault exists in said integrated circuit, the input/output signals of said circuit are transferred to their designated path.

4. The yield enhancement circuit of claim 1 wherein if the fault indication device is activated indicating existence of a faulty circuit and the redundancy implementation signal indicates that the fault exists in said integrated circuit, the input/output signals of said adjacent sub-circuit are transferred to the designated path.

5. The yield enhancement circuit of claim 1 wherein the integrated circuit is a memory.

6. The yield enhancement circuit of claim 5 wherein the memory is selected from the set of memories comprising static random access memory, dynamic random access memory, non-volatile random access memory.

7. The yield enhancement circuit of claim 5 wherein each of the sub-circuits comprises a column of memory cells and a read/write buffer connected to the column of memory cells.

8. The yield enhancement circuit of claim 1 wherein the designated path is an input/output driver/receiver circuit that transfers the input/output signals from/to external circuitry.

9. The yield enhancement circuit of claim 1 wherein each fault indication device comprises a fuse, whereby when said fuse is intact, said sub-circuit does not contain the fault and when said fuse is not intact, said sub-circuit contains the fault.

10. The yield enhancement circuit of claim 9 wherein each fault indication device further comprises a logical combining circuit to logically combine each fault signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent sub-circuits.

11. A yield enhancement circuit within a memory integrated circuit for substituting redundant groups of memory cells for faulty groups of memory cells within said memory integrated circuit, comprising:

a plurality of fault indication devices, wherein each fault indication device is associated with one group of memory cells of the memory integrated circuit such that one fault indication device is activated to generate a fault signal to express existence of a fault within the faulty group of memory cells of said memory integrated circuit, additionally each fault indication device that is associated with a selected adjacent group of memory cells of the memory integrated circuit generates the fault signal to express the existence of the fault within the faulty group of memory cells of said memory integrated circuit;

a fault detection device in communication with the plurality of fault indication devices to determine the existence of the faulty group of memory cells within the memory integrated circuit and transmit a redundancy implementation signal upon determination of existence of the faulty group of memory cells; and

a plurality of redundancy activation circuits in communication with the fault detection device to receive the redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the group of memory cells to which said fault indication device is associated and associated to an adjacent group of memory cells of said group of memory cells to which said fault indication device is associated to selectively transfer input/output signals of the group of memory cells associated with the

fault indication device and its adjacent group of memory cells to a designated path dependent on the expression of the existence of a fault within the memory integrated circuit.

12. The yield enhancement circuit of claim 11 wherein if the fault indication device is not activated indicating that the associated group of memory cells has no fault and the redundancy implementation signal indicates that no fault exists in said memory integrated circuit, the input/output signals of said circuit are transferred to their designated path.

13. The yield enhancement circuit of claim 11 wherein if the fault indication device is not activated indicating that the associated circuit has no fault, but the redundancy implementation signal indicates that the fault exists in said memory integrated circuit, the input/output signals of said circuit are transferred to their designated path.

14. The yield enhancement circuit of claim 11 wherein if the fault indication device is activated indicating existence of a faulty group of memory cells and the redundancy implementation signal indicates that the fault exists in said memory integrated circuit, the input/output signals of said adjacent group of memory cells are transferred to the designated path.

15. The yield enhancement circuit of claim 11 wherein the memory integrated circuit is selected from the set of memory integrated circuits consisting of static random

access memory, dynamic random access memory, and non-volatile random access memory.

16. The yield enhancement circuit of claim 15 wherein each of the group of memory cells comprises a column of memory cells and a read/write buffer connected to the column of memory cells to selectively sense data stored in said column of memory cells and to store data to said column of memory cells.

17. The yield enhancement circuit of claim 11 wherein the designated path is an input/output driver/receiver circuit that transfers the input/output signals from/to external circuitry.

18. The yield enhancement circuit of claim 11 wherein each fault indication device comprises a fuse, whereby when said fuse is intact, said group of memory cells does not contain the fault and when said fuse is not intact, said group of memory cells contains the fault.

19. The yield enhancement circuit of claim 18 wherein each fault indication device further comprises a logical combining circuit to logically combine each fault signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent group of memory cells.

20. A memory comprising:

at least one array of memory cells, each array of memory cells arranged in rows and columns of memory cells;

at least one redundant column of memory cells associated with at least one of said arrays of memory cells to replace a faulty column of memory cells; and

a yield enhancement circuit in communication with at least one array of said memory cells and said redundant columns of memory cells for substituting redundant column of memory cells for a faulty column of memory cells within said associated arrays of memory cells, said yield enhancement circuit comprising:

a plurality of fault indication devices, wherein each fault indication device is associated with one column of memory cells of the arrays of memory cells such that one fault indication device is activated to generate a fault signal to express existence of a fault within the faulty column of memory cells of said arrays memory cells, additionally each fault indication device that is associated with a selected adjacent column of memory cells of the arrays of memory cells generates the fault signal to express existence of the fault within the faulty column of memory cells of said arrays of memory cells;

a fault detection device in communication with the plurality of fault indication devices to determine the existence of the faulty column of memory cells within the arrays of memory cells and transmit a

redundancy implementation signal upon determination of existence of the faulty column of memory cells; and

a plurality of redundancy activation circuits in communication with the fault detection device to receive the redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the column of memory cells to which said fault indication device is associated and associated to an adjacent column of memory cells of said column of memory cells to which said fault indication device is associated to selectively transfer input/output signals of the column of memory cells associated with the fault indication device and its adjacent column of memory cells to a designated path dependent on the expression of the existence of a fault within the arrays of memory cells.

21. The memory of claim 20 wherein if the fault indication device is not activated indicating that the associated column of memory cells has no fault and the redundancy implementation signal indicates that no fault exists in said arrays of memory cells, the input/output signals of said circuit are transferred to their designated path.

22. The memory of claim 20 wherein if the fault indication device is not activated indicating that the associated circuit has no fault, but the redundancy implementation signal indicates that the fault exists in said arrays of memory

cells, the input/output signals of said circuit are transferred to their designated path.

23. The memory of claim 20 wherein if the fault indication device is activated indicating existence of a faulty column of memory cells and the redundancy implementation signal indicates that the fault exists in said arrays of memory cells, the input/output signals of said adjacent column of memory cells are transferred to the designated path.

24. The memory of claim 20 wherein the arrays of memory cells are selected from the set of arrays of memory cells consisting of static random access memory cells, dynamic random access memory cells, and non-volatile random access memory cells.

25. The memory of claim 24 wherein each of the column of memory cells comprises a column of memory cells and a read/write buffer connected to the column of memory cells to selectively sense data stored in selected memory cells and to store data to said selected memory cells.

26. The memory of claim 20 wherein the designated path is an input/output driver/receiver circuit that transfers the input/output signals from/to external circuitry.

27. The memory of claim 20 wherein each fault indication device comprises a fuse, whereby when said fuse is intact, said column of memory cells does not contain

the fault and when said fuse is not intact, said column of memory cells contains the fault.

28. The memory of claim 27 wherein each fault indication device further comprises a logical combining circuit that logically combine each fault signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent column of memory cells.

29. A method for yield enhancement of an integrated circuit by substituting a redundant circuit for a faulty circuit of said integrated circuit, comprising the steps of:

providing fault indication associated with each sub-circuit of the integrated circuit such that one fault indication generates a fault signal to express the existence of a fault within the faulty circuit of said integrated circuit, additionally each fault indication associated with selected adjacent sub-circuits of the integrated circuit generates the fault signal to express the existence of the fault within the faulty circuit of said integrated circuit;

determining the existence of the faulty circuit within the integrated circuit from said fault signal;

generating a redundancy implementation signal upon determination of existence of the faulty circuit; and

initiating redundancy activation upon generating the redundancy implementation signal and one of the fault indications associated with the sub-circuit to selectively transfer input/output signals of the sub-circuit associated with the fault indication and an adjacent sub-circuit to a designated path dependent on the expression of the existence of a fault within the integrated circuit.

30. The method of claim 29 wherein if the fault indication is not activated indicating that the associated sub-circuit has no fault and the redundancy implementation signal indicates that no fault exists in said integrated circuit, the input/output signals of said circuit are transferred to their designated path.

31. The method of claim 29 wherein if the fault indication is not activated indicating that the associated sub-circuit has no fault, but the redundancy implementation signal indicates that the fault exists in said integrated circuit, the input/output signals of said circuit are transferred to their designated path.

32. The method of claim 29 wherein if the fault indication is activated indicating existence of a faulty circuit and the redundancy implementation signal indicates that the fault exists in said integrated circuit, the input/output signals of said adjacent sub-circuit are transferred to the designated path.

33. The method of claim 29 wherein the integrated circuit is a memory.

34. The method of claim 34 wherein the memory is selected from the set of memories comprising static random access memory, dynamic random access memory, non-volatile random access memory.

35. The method of claim 36 wherein each of the sub-circuits comprise a column of memory cells and a read/write buffer connected to the column of memory cells.

36. The method of claim 29 wherein the designated path is an input/output driver/receiver circuit that transfers the input/output signals from/to external circuitry.

37. The method of claim 29 wherein each fault indication is generated by a fuse, whereby when said fuse is intact, said sub-circuit does not contain the fault and when said fuse is not intact, said sub-circuit contains the fault.

38. The method of claim 37 wherein each fault indication further generates a logical combining circuit that logically combines each fault indication with the fault indication that is associated with selected adjacent sub-circuits.